In the Claims

1. (Currently amended) A method of manufacturing a field electron emission cathode having at least one cathode electrode which comprises a field emitting layer (302) on a ~~betewwn~~ first ~~and second~~ conducting layer[[s]] (301[[303]]), and at least one gate electrode which overlies said cathode electrode and comprises an insulating layer (304) and a ~~third~~ gate conducting layer (305), characterised in that said method comprises the steps of:

a. depositing on an insulating substrate (300) to form by low resolution means, a sequence of said first conducting layer (301), said field emitting layer (302) and an etch-stop ~~second conducting~~ layer (303) to form said at least one cathode electrode;

b. depositing on said cathode electrode to form by low resolution means, a sequence of said insulating layer (304) and ~~third~~ gate conducting layer (305), to form said at least one gate electrode;

c. coating the structure thus formed with a photoresist layer (306);

d. exposing said photoresist layer (306) by high resolution means to form at least one group of emitting cells, the or each said group being located in an area of overlap between one said cathode electrode and one said gate electrode;

e. etching sequentially said ~~third~~ gate conducting layer (304), said insulating layer (304) and said ~~second conducting~~ etch-stop layer (303) to expose said field emitting layer (302) in said cells, such that said etch-stop layer (303) protects said field emitting layer (302) from etchant during etching of said insulating layer (304); and

f. removing remaining areas of said photoresist layer (306).

2. (Original) A method according to claim 1, wherein said cathode is a cathode array, said cathode electrode and said gate electrode comprise respectively cathode addressing tracks and gate addressing tracks, which tracks are arranged in addressable rows and columns, and step d. includes forming a pattern of said groups of emitting cells.

3. (Original) A method according to claim 2, wherein at least one of or all of said cathode addressing tracks address(es) a plurality of rows or columns of cells.

4. (Previously presented) A method according to claim 2, wherein said steps of exposing and etching include the formation of fiducial marks (432) on the cathode array, to facilitate the subsequent alignment of the array with an anode or other component after manufacture of the array.

5. (Currently amended) method according to claim 1, 2, 3 or 4, comprising the step of forming at least one of said conducting layers (301, [[303,]] 305) by application of a liquid bright metal or by electroless plating.

6. (Currently amended) A method according to claim 1, 2, 3 or 4, comprising the step of forming at least one of said conducting layers (301, [[303,]]305) by a means other than vacuum evaporation or sputtering.

7. (Currently amended) A method according to claim 1, 2, 3 or 4, wherein said field emitting layer (302) comprises a layer of broad area field emitter material.

8. (Currently amended) A method according to claim 1, 2, 3 or 4, comprising the further steps of depositing sequentially a second insulating layer (606) and ~~fourth~~ focus conducting layer (607) onto the cathode after completion of steps a. to f., to form a focus grid.

9. - 15. (Cancelled)

16. (New) A method according to claim 1, 2, 3 or 4, wherein said etch-stop layer (303) is a conducting layer.

17. (New) A method according to claim 1, 2, 3 or 4, wherein said etch-stop layer (303) is a metal layer.